REMARKS

Claims 1-29, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 4-6, 8-11, 14-16, 18-21, 24-26, 28-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Dutton et al., hereinafter "Dutton" (U.S. Patent No. 6,047,350); and claims 2-3, 7, 12-13, 17, 22-23, and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dutton. Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejections Based on Dutton

Applicants submit that the claimed invention is patentable over Dutton principally because the claims define a bridge that has channels that are uniquely dedicated to different devices, while Dutton merely describes a conventional bridge 106 and does not teach or suggest that that bridge 106 has multiple channels, much less that the channels are uniquely dedicated to different devices. For example, the only discussion of the features of the bridge within Dutton appear in column 4, line 15-48, and that portion of Dutton does not describe that the bridge 106 has multiple channels, nor does it describe that the bridge 106 dedicates specific channels to specific devices.

More specifically, independent claim 1 defines that the "bridge includes a first channel dedicated to said processor local bus . . . a second channel dedicated to said peripheral device bus . . . a third channel dedicated to said memory unit; and . . . a fourth channel dedicated to said input/output unit." Additionally, independent claim 10 defines that the bus, memory unit, and input/output unit are each "connected to a uniquely dedicated channel in said bridge." Further, independent claim 20 defines a bridge that

has "dedicated channels each uniquely connected to one or more of:" the bus, memory unit, input/output unit, and peripheral device.

Most shared bus system interfaces, such as the one shown in Dutton, are inherently blocking, because of their handshaking protocol. This limits the effectiveness of today's high-performance embedded processors in several ways. To improve performance, the invention provides the system architecture shown in Applicants' Figures 2-4 that addresses communication related performance bottlenecks.

The invention provides non-blocking communication through multiple reserved lanes in the bridge (e.g., channels 319-325) that are managed by an implicit protocol (e.g., buffers 314 and multiplexors 316). The invention avoids relying on handshaking signals that leads to blocking communications when a destination or a shared resource is overloaded. The virtual channel communication architecture (VCCA), shown in Applicants' Figures 2-4, provides application specific bus interface flow control, by coordinating the access of resource competing components using reserved lanes. The virtual channel scheduler module uses multiple FIFO buffers 314, dedicated to distinct virtual channels 319-325, to allow the invention to implement the required multiple reserved lanes. With the invention, transactions occurring on each port interface may be routed to adjacent ports without having to pass through a bus. Similarly, each port has a data-path dedicated to the processor local bus 206.

For systems interconnected through a shared bus interface, when more than two bus masters are active, the effective bandwidth of each access is significantly reduced compared to the maximum bandwidth observed when only one bus master is active. Furthermore, if concurrent accesses are not coordinated, one or more bus master may incur an unacceptable latency due to busy wait signals. This latency is even longer when access is required across a bus bridge. By adding hardware support for non-blocking inter-virtual component communication, in the form of the VCCA bridge 230, the claimed invention improves the performance of embedded systems. Such performance gains allow concurrent computations to utilize nearly all the available bus bandwidth while satisfying real-time requirements through the use of dedicated channels for each interface. The claimed bridge provides a performance boost on embedded systems in which there are contentions for communication resources (e.g. shared bus bandwidth,

FIFO buffer) among application components. Furthermore, the claimed bridge's ability to exploit a large processor local bus bandwidth is relatively independent of the processor's access pattern or the number of streams in a given computation. The claimed bridge configured with appropriate FIFO 314 depths, can generally exploit the full available processor local bus bandwidth.

To the contrary, Dutton merely describes a conventional bridge 106 and does not explain any details about the bridge 106. More specifically, in column 4, lines 15-48, Dutton describes that the chipset logic 106 includes various bridge logic and includes arbitration logic 107. The chipset logic 106 is similar to the Triton chipset available from Intel Corporation, including certain arbiter modifications to accommodate the real-time bus of the present invention. A second level or L2 cache memory may be coupled to a cache controller in the chipset logic 106, as desired. The bridge or chipset logic 106 couples through a memory bus 108 to main memory 110. The chipset logic 106 includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107. The chipset logic 106 includes various peripherals, including an interrupt system, a real time clock (RTC) and timers, a direct memory access (DMA) system, and ROM/Flash memory. Other peripherals are comprised in the chipset logic 106, including communications ports, diagnostics ports, command/status registers, and non-volatile static random access memory (NVSRAM). The host/PCI/cache bridge or chipset logic 106 also interfaces to a local expansion bus or system bus 120.

The only discussion of different byte channels in Dutton relates to the multimedia devices 142-146. More specifically, in column 6, lines 10-31, Dutton describes the byte slicing logic that efficiently uses each data byte channel of the bus. However, this discussion only relates to the multimedia devices and does not relate to the bridge. To the contrary, there is no discussion in Dutton regarding the bridge 106 having multiple channels, much less each channel being uniquely dedicated to a different bus, memory unit, input/output unit, peripheral device, etc.

Therefore, it is Applicants position that Dutton does not teach any details regarding the bridge 106 and therefore does not teach or suggest that the "bridge includes a first channel dedicated to said processor local bus . . . a second channel dedicated to said peripheral device bus . . . a third channel dedicated to said memory unit; and . . . a

fourth channel dedicated to said input/output unit," as defined by independent claim 1; that the bus, memory unit, and input/output unit are each "connected to a uniquely dedicated channel in said bridge"; as defined by independent claim 10; or a bridge that has "dedicated channels each uniquely connected to one or more of:" the bus, memory unit, input/output unit, and peripheral device, as defined by independent claim 20 . Therefore, Applicants submit that independent claims 1, 10, and 20 are patentable over the prior art record. Further, dependent claims 2-9, 11-19, and 21-29 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention defined. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-29, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

09/708,494

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 7/30/03

Frederick W. Gibb, III
Reg. No. 37,629

McGinn & Gibb, PLLC
2568-A Riva Road
Suite 304
Annapolis, MD 21401
(301) 261-8071
Customer Number: 29154